# A Review on Low Power Design of Integrated Circuits

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## ABSTRACT

*Integrated Circuits were invented a long back but as the technology is progressing, it has been realized that there is a need of low cost, low power and high-performance applications from a variety of consumer. Leakage current plays major role in CMOS technologies. In CMOS technologies two types of power dissipation are dynamic power dissipation and static power dissipation. Aim of this paper is to elaborate recent trends in low power design along with the evolution of new technologies. This paper reviews low power design techniques of integrated circuits and some reviews regarding components of the power dissipation in integrated circuit is also presented.*

***Keywords - Leakage Power, Low-power, Power Dissipation, CMOS Technologies***

## 1. INTRODUCTION

Electronic devices and there different system are now part of every human life. Almost all the devices are battery operated as well as are portable. These devices have come a long way from requiring huge power house, to a micro hand held battery used for the application of devices like a palmtop. Portable electronic devices require integrated circuits to operate under consumption of low power [8]. ICs which operates under low-power demand has high performance. From market perspective these incredible qualities are required on moderate to low cost with more developed features. Because of these reasons a new research from a micrometer level to nanometer level [3]. When the vertical and lateral dimensions are scaled down and voltage of MOS transistors are increased, the overall power dissipation of chip is decreased and also reduce the chip area, hence deducting the cost of each transistor.

The method which is used for the scaling of CMOS is: Full scaling or Constant field scaling, generalized scaling, and constant voltage scaling.

## 2. POWER CONSUMPTION COMPONENTS OF CMOS

### 2.1 DYNAMIC POWER CONSUMPTION (Pd)

This component is because of logic gates switching activity in the circuit of CMOS. Gates continuously charge and then the load capacitances get discharge [3] as per logic-switching activity. The power consumed in it depends on switching frequency, switching node capacitance and power supply voltage.

### 2.2 LEAKAGE POWER ($P_{LEAK}$) CONSUMPTION / STATIC DC POWER

When device is in "OFF" state, static power occurs. For digital application, MOS transistors act like switches [2]. When the device is in static and switching mode it consumed leakage power, but the main concern of leakage power is when device is in the inactive state, and power consumed that state is considered as "wasted" power [7]. Main causes for the consumption of leakage power are reverse bias current, sub threshold channel leakage current, drain induced barrier lowering leakage, gate induced drain leakage, punch throw, narrow width effect, gate oxide tunneling current, and hot carrier injection current are shown in Fig. 1

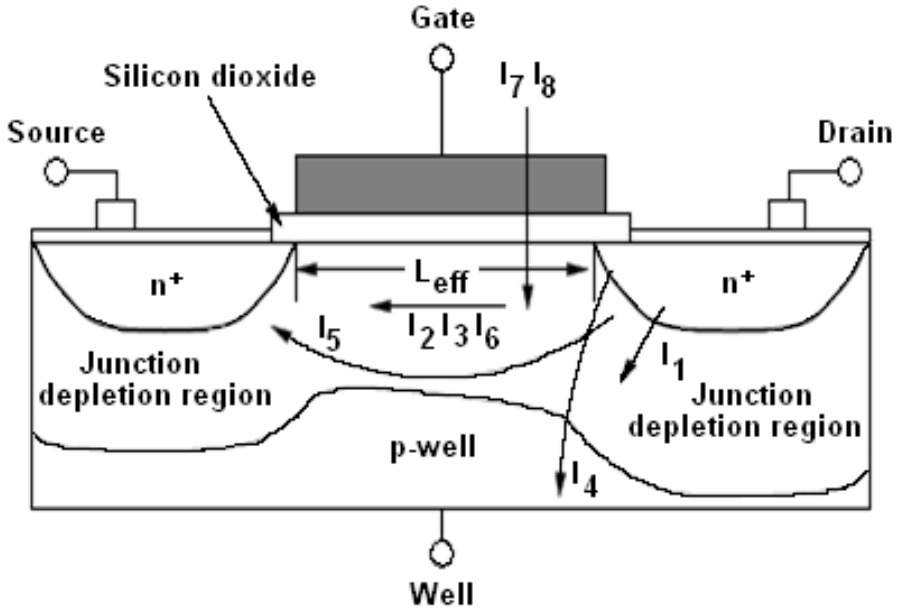


Fig.1 Leakage Current Mechanism in A Short-Channel NMOS Transistor

Where
$I_1$ - Reverse Diode Leakage Current
$I_2$ - Sub threshold Leakage Current
$I_3$ - Drain Induced Barrier Lowering Effect
$I_4$ - Gate Induced Drain Leakage
$I_5$ - Punch through
$I_6$ - Narrow Channel Effect
$I_7$ - Gate Oxide Tunneling
$I_8$ - Hot Carrier Injection

### 2.3 SHORT CIRCUIT POWER CONSUMPTION ($P_{SC}$)

Fig.2 shows, in the static CMOS circuits, the path of short-circuit exists for direct current flow from VDD to ground, when
VTn< Vin< VDD-|VTp|

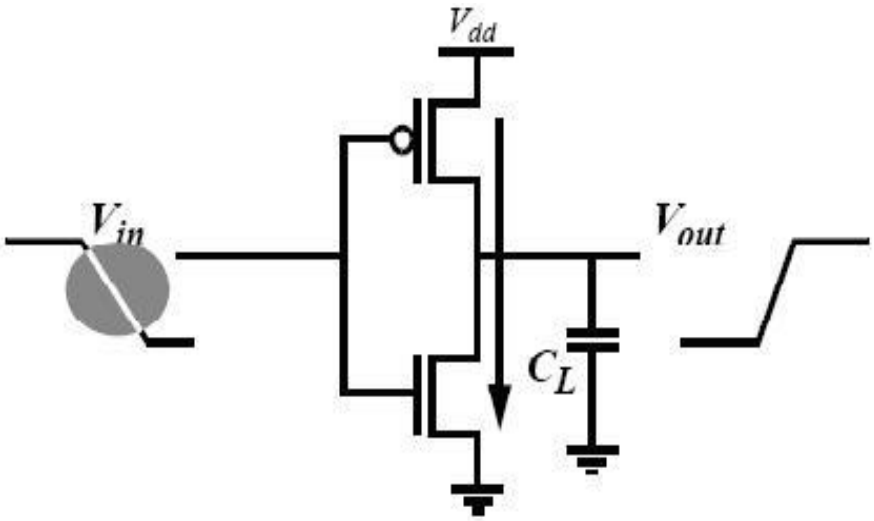


Figure 2: Short Circuits Power in CMOS Circuit

## 3. LOWERING POWER CONSUMPTION APPROACHES

Power consumption is needed at both the level i.e. circuit design level and at the technological level [6]. Application with ultra low power level, it is mandatory now that innovations in circuit design techniques for each level of abstractions along with optimization is necessary.

### 3.1 WAYS TO REDUCE $P_D$ (DYNAMIC POWER)

Dynamic Power gradually depends on the $V_{DD}$. Hence, if we reduce $V_{DD}$ it will lead to the reduction of $P_D$ [4]. As $V_{DD}$ should be compatible with the chip which is assembled within the system, so the $V_{DD}$ cannot be minimized arbitrarily [1]. After an argument between VLSI Industries on global level, power supply voltage for CMOS technologies has been reduced.

Few circuit designs acquire multiple type of power supply. So they retain high $V_{DD}$ for the critical path circuits and also generate low supply voltage for the blocks that are power sensitive. Table 1 shows the $V_{DD}$ Scaling Scenario [3].

Table.1- $V_{DD}$ Scaling Scenario

| Year of Introduction | 1974 | 1984 | 1994 | 2004 |
|---|---|---|---|---|
| Power Supply ($V_{DD}$) | 10 V | 5 V | 3.5 V | 1 V |
| Technology Mode | 5 micrometer | 1 micrometer | 0.35 micrometer | 90 nanometer |

### 3.2 WAYS TO REDUCE $P_S$ (STATIC POWER)

Static power of CMOS depends on $V_{DD}$ and $I_{Leak}$ [3]. So when we reducing $V_{DD}$ static power reduce. We can also reduced $I_{Leak}$ in the application of ultra power [5].

Four leakage current components are i.e. sub threshold leakage current ($I_{SUB}$), Junction leakage current ($I_J$), gate leakage current ($I_{GATE}$) and Gate Induced Drain leakage current ($I_{GIDL}$).

## 4. NEW TECHNOLOGIES FOR HIGH PERFORMANCE OF ULTRA LOW POWER

Previous section shows by reducing $V_{DD}$ power consumption reduces and also reliability problem suppresses. Power goal and performance of certain application in advanced nodes of 32 nm and 40 nm etc is not achieved with CMOS process. So it has led new technologies are Silicon – on – Insulator (SOI) and FINFET.

## 5. CONCLUSION

For high performance demand with the low consumption has been surged, this has led the Scaling of CMOS from micrometer (mm) to nanometer (nm) ranges. Conventional CMOS technologies cannot meet these requirements, so the new technology was invented. This paper has deal in detail the power consumption components in CMOS and reviewed the methodologies to drive for the low power consumption.

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